

Physical 3D Single Event Upset Simulation of a SRAM Cell with Victory and SmartSpice SEE

Introduction

Victory simulation framework includes tools for 1D, 2D and 3D simulation of modern semiconductor technologies. Victory implements a full tetrahedral meshing engine for fast and accurate simulation of complex 3D geometries. Built-in and user defined mesh refinement criteria can be used for customization of the mesh during a simulation. This is the case, for example for Single Event Upset (SEU) simulation. The simulation of SEU phenomena in 3D structures is highly complicated due to the presence of large gradients in physical quantities near the SEU track. In order to perform accurate and stable simulations of SEU strikes in 3D structures, it is essential to have fairly dense mesh near the center of the SEU track while maintain a coarser mesh far from the track for efficiency.

The aim of this paper is to illustrate how a SRAM cell subject to SEU can be accurately simulated.

Creation of the Structure

A three-dimensional structure composed of 2 NMOS and 2 PMOS is created with DevEdit 3D. Using capabilities of

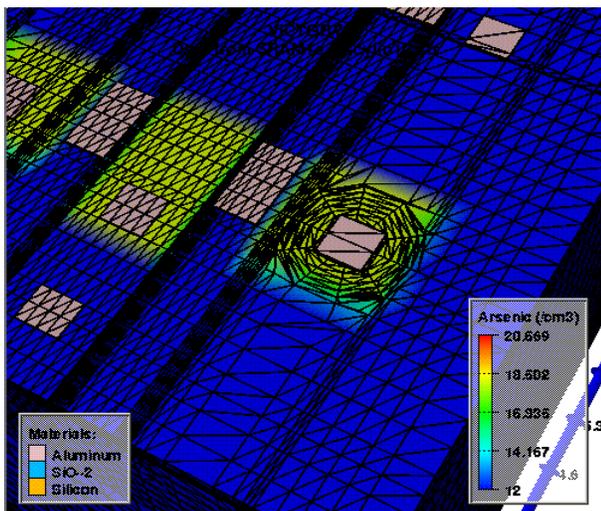


Figure 1. Arsenic concentration and surface mesh of the SRAM structure

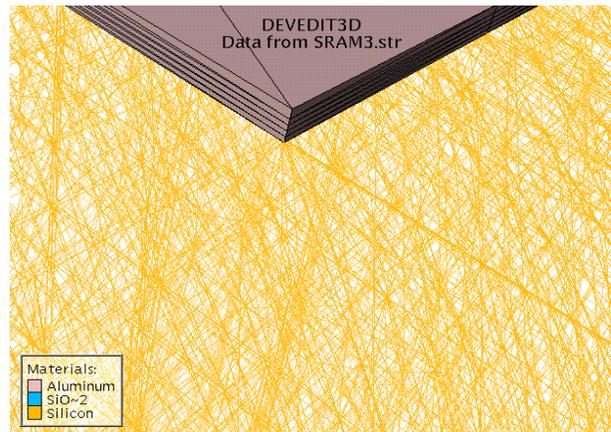


Figure 2. Tetrahedral mesh around a contact of the SRAM structure.

DevEdit 3D, geometry, materials, concentration contours and 3D tetrahedral mesh of the structure is done for the subsequent device simulation. Doping and surface mesh of the three-dimensional structure is shown in Figure 1. It is very important to notice that cylindrical remesh has been done where the strike will be applied. Tetrahedral elements of the three-dimensional structure are also shown in Figure 2 with a zoom around a contact.

A schematic diagram of a 4 transistors SRAM circuit is shown in Figure 3. The 4 transistors are used for numerical device simulation. Thus all the coupling effects between transistors are taken into account. No transistor in the SRAM circuit is simulated as SPICE device.

Simulation

Simulation inputs to Victory are defined in DeckBuild including the following (Figures 4 and 5):

- Devedit structure loading
- Cylindrical remesh
- Models specification
- DC and transient analysis specifications

The orientation of the single event upset strike is specified by a pair of (x,y,z) ordinates corresponding to the entry and exit locations (Figure 6).

The single event upset track is assumed to be cylindrical, and the location of the peak charge density in time can be specified along with the width (in time) of the charge generation pulse. A default SEU function exists in Victory but any user-defined strike function can be created (Figure 7).

The specified DC biasing of the SRAM circuit sets nodes three and two to 0.0 and 3.3 V respectively. The DC biasing on the SRAM circuit is used as the initial condition for the transient analysis. The transient analysis is carried out for ten microseconds with an initial time step of ten femtoseconds. The SEU strike has a maximum density at 4 picoseconds and a width of two picoseconds.

Results

Victory simulation outputs provide the node voltages and currents as a function of the transient time. Additionally the internal device behavior (e.g., potential and electron concentration) can be analyzed as a function of the transient time.

A plot of the voltages at nodes two and three versus transient time shows how these voltages are affected by the incoming single event upset particle (Figure 8).

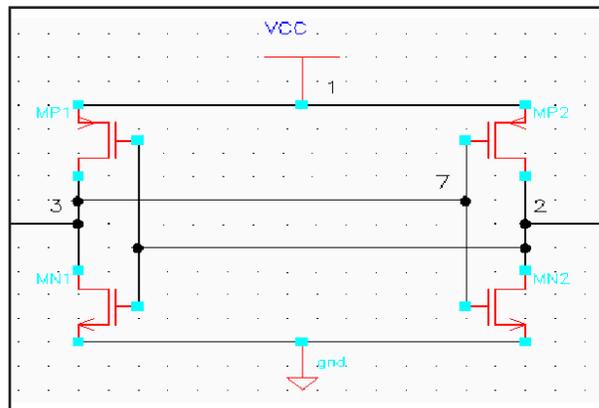


Figure 3. Schematic of the SRAM cell.

Without cylindrical mesh refinement along the strike the simulation result is incorrect (blue curves in Figure 9) since voltages remain flat. In Figure 9, green curves and red curves correspond to a mesh refinement along the track with 2 and 10 cylinders respectively.

A plot of the mesh discretization factor is done in 2D along the strike when cylindrical remesh has been done using 2 or 10 cylinders (Figure 10). This mesh discretization factor helps the user to locate the area where the mesh has to be refined. Red indicates the most nonlinear elements (on a relative linear scale), which means that these regions are the ones where refinement will probably make the largest difference in the solution.

```

Deckbuild V3.23.17.R -- (NONE) (edited), dir: /home/eric/worki
File View Edit Find Main Control Commands Tools
solve vgate=0.1 vstep=0.1 vstop=3.3 name=gate
solve vsource=0.1 vstep=0.1 vstop=3.3 name=source

# contact definition
contact name=source current
contact name=bulk current
contact name=drain current COMMON=bulk WORK=4.35
contact name=substrate current COMMON=source WORK=4.35
contact name=fgate current COMMON=source WORK=4.25
contact name=base current COMMON=bulk WORK=4.25
contact name=anode current COMMON=source
contact name=vss COMMON=gate
contact name=vgg COMMON=collector
contact name=cgate current COMMON=bulk

models consrh auger bgn cvt klassen
method bicgst.rcm
method linear.Fill_level=2
method linear.scaling_parameter=2

solve isource=0
solve ibulk=0

beam f.radiate=ion_c_inter_v_LET_3.5.lib
log outf=SRAM.log
solve tfinal=1e-5 tstep=1.e-14
    
```

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Executing on host: triesves

Starting: DEVICE module.

VICTORY>

VICTORY started VICTORY

Figure 5. Models, DC and transient analysis specifications

```

Deckbuild V3.23.17.R -- (NONE) (edited), dir: /home/eric/worki
File View Edit Find Main Control Commands Tools
go victory
mesh inf=SRAM.str hybridx

contact NAME=gate
contact NAME=source
contact NAME=bulk
contact NAME=drain WORK=4.35 COMMON=bulk
contact NAME=substrate WORK=4.35 COMMON=source
contact NAME=fgate WORK=4.25 COMMON=source
contact NAME=collector
contact NAME=base WORK=4.25 COMMON=bulk
contact NAME=anode COMMON=source
contact NAME=vss COMMON=gate
contact NAME=vgg COMMON=collector
contact NAME=cgate COMMON=bulk

models consrh auger bgn cvt klassen
method bicgst.rcm
method linear.Fill_level=2
method linear.scaling_parameter=2

method NONLINEAR.MAX_ITERATIONS=30

regrid x,min=0.775 y,min=0 z,min=3.22 \
x,max=0.775 y,max=5 z,max=3.22 \
radius=0.05 \
lmax=20 rmax=10 num.cylinders=10 constraint
    
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Starting: DEVICE module.

VICTORY>

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Figure 4. DevEdit structure loading and cylindrical remesh definition

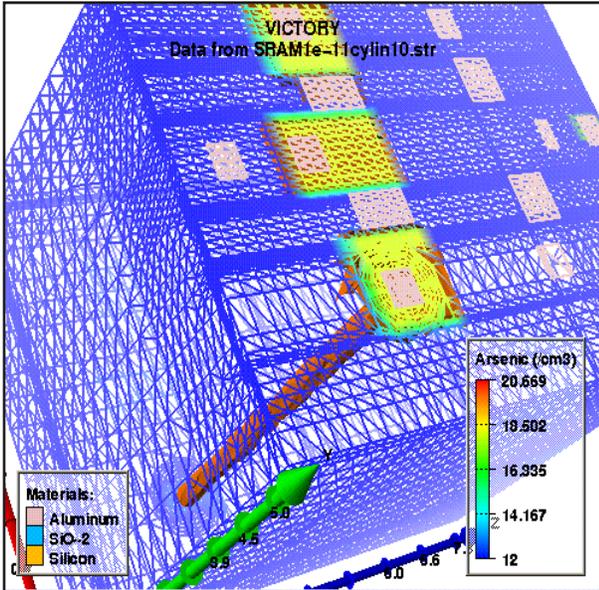


Figure 6. 3D SRAM structure showing the location of the strike.

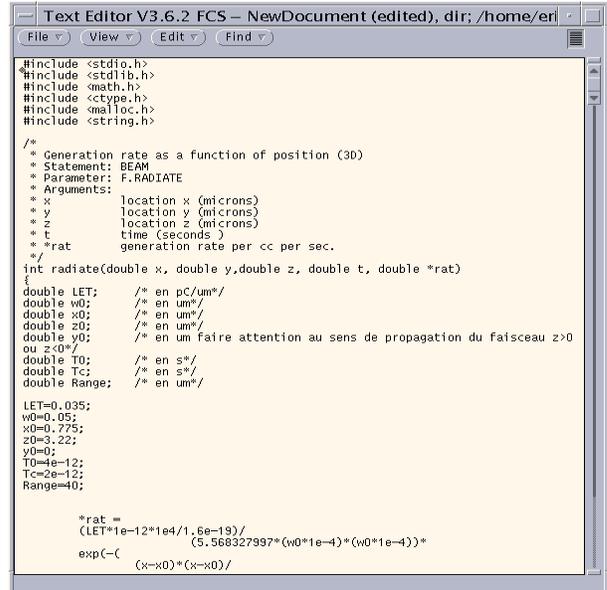


Figure 7. User defined strike function using C-Interpreter.

As a conclusion, the mesh refinement using only 2 cylinders is probably just enough to get an accurate result.

A plot of the voltages at nodes two and three versus transient time is shown depending of the intensity of the strike (Figure 11). Thus the behavior of the SRAM cell can be analyzed as a function of the intensity of the strike. For a low intensity (blue curves), the SRAM remains un-

changed. With a medium intensity (green curves) voltages switch. Finally for a high intensity (red curves), the SRAM becomes unstable.

Three-dimensional electron current density contours can be used to follow the evolution of the electron current density in the impacted NMOSFET as the SRAM cell experiences the upset. Initially, a low electron current density

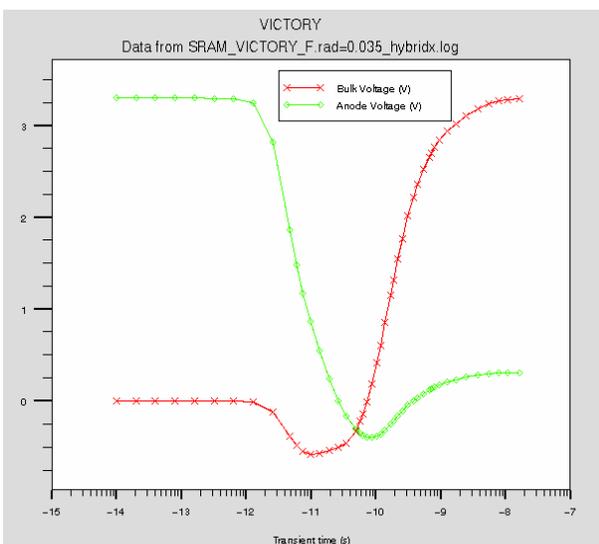


Figure 8. Voltages at nodes 2 and 3 (see Figure 3) versus transient time. The anode voltage corresponds to node 2 and the bulk voltage to node 3.

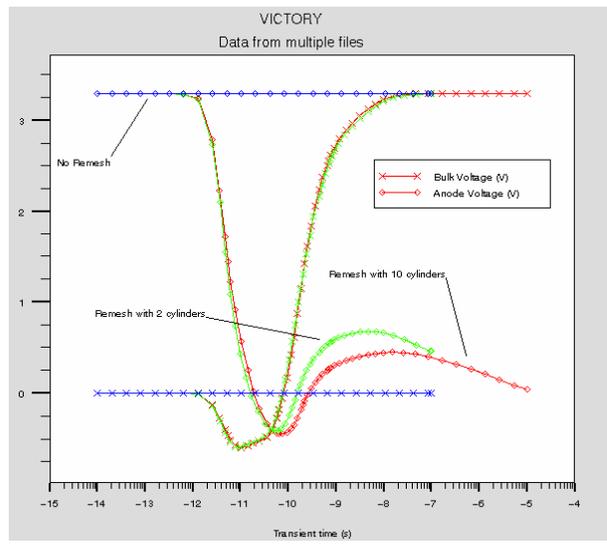


Figure 9. Voltages at nodes 2 and 3 (see Figure 3) versus transient time and density of the mesh along the track. The anode voltage correspond to node 2 and the bulk voltage to node 3.

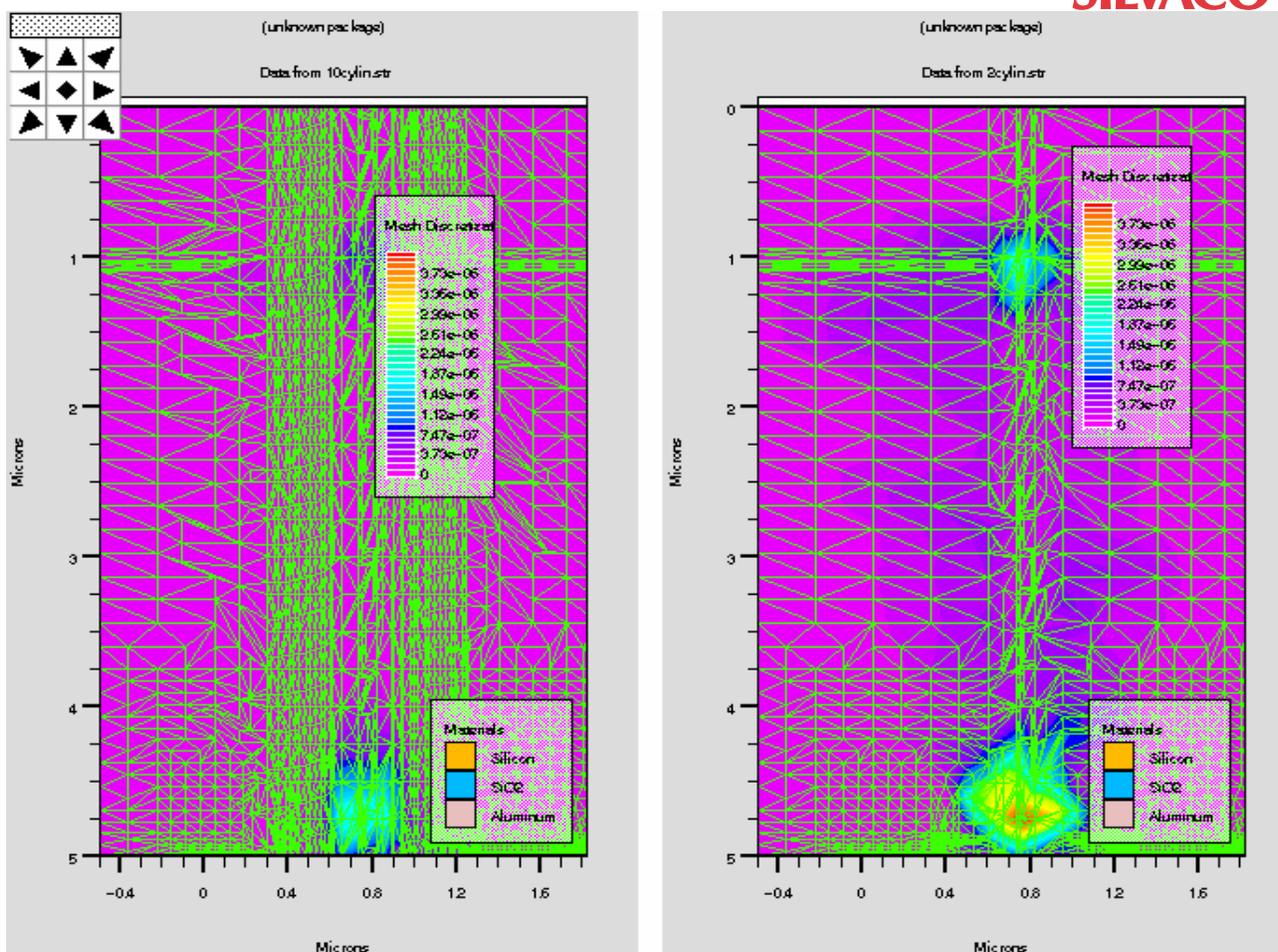


Figure 10. Mesh discretization factor at node 3 using 2 cylinders (Left) and 10 cylinders (Right).

flows between the source and drain regions of the NMOS-FET (the transistor is off). As the SEU strike enters the NMOSFET, electron-hole pairs are created along the SEU strike path, altering the electron distribution throughout the device and thus increasing the electron current density in the NMOSFET (the transistor is on) (Figure 12). As the SEU strike exits the structure, the external charge source is removed and the original electron current density is re-established (the transistor is off again).

5. Circuit Simulation

As previously described it is very interesting to be able to analyze in details the behavior of transistors or circuits composed by a small numbers of transistors by using TCAD simulation. Indeed one can have access to quantities like potential, electron concentration, current density that allow the user to study in details the behavior of the impacted devices. However when we want to study the SEU impact on larger circuits, TCAD simulation is no more possible. This is why SmartSpice SEE module

was developed to accurately simulate SEE (Single Event Effect) in MOS (Bulk and SOI) and in Bipolar devices. The impact of incident particles induces a generation of hole-electron pairs. A current generator is inserted in the circuit to model the charge collected on an assumed susceptible node as a result of the particle hit. For ASICs, the sensitive nodes can be localized. The shape of the generated current is closely approximated by double-exponential source available in SmartSpice. Other waveforms are also available in SmartSpice.

A plot of the voltages of a latch circuit versus transient time shows how these voltages are affected by the incoming single event upset particle (Figure 13).

Figure 13 shows the stable state of the latch (top figure), then the influence of an impact at t=10ns (middle figure). The effect produces only a parasitic effect without affecting the state of the latch. When increasing the energy (LEF), the impact changes the state of the latch and produces an error in the circuit (bottom figure).

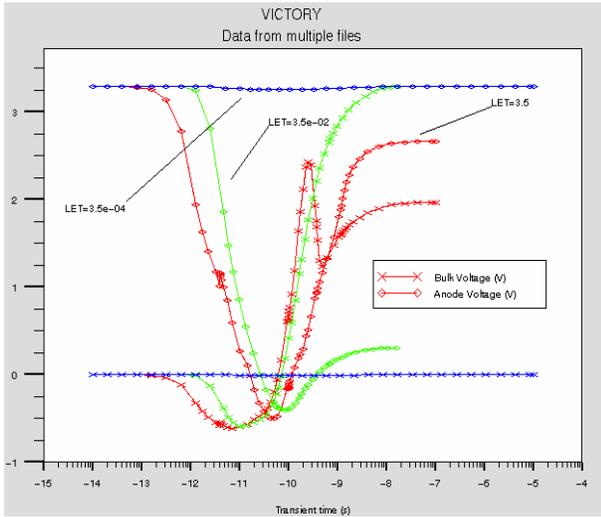


Figure 11. Voltages at nodes 2 and 3 (see Figure 3) versus transient time and intensity of the strike. The anode voltage correspond to node 2 and the bulk voltage to node 3

SmartSpice SEE is able to simulate multiple impacts at the same time or at different time on different nodes of the circuit. The user can personalize the upset detection with absolute or relative threshold on any nodes at the same time. The Critical charge (QCRIT), which causes a change of state, can be automatically computed. Please refer to the SmartSpice SEE documentation for more details.

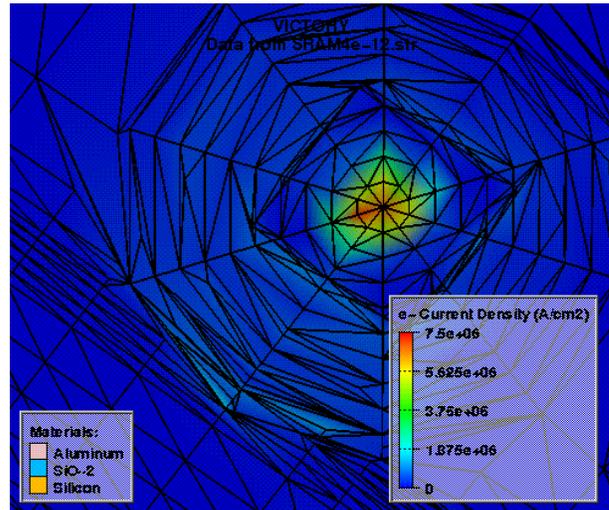


Figure 12. Current density at the drain of NMOS Transistor (node 3) at $t=4e-12s$

6. Conclusion

We have demonstrated that IV curves from Victory account for the SEU strike charge generation thanks to specific meshing capabilities and accurate physical models. The current profile from Victory can be fitted to a SmartSpice current source, which then allows the SEU upset of any type of circuits to be predicted by using SmartSpice SEE capabilities.

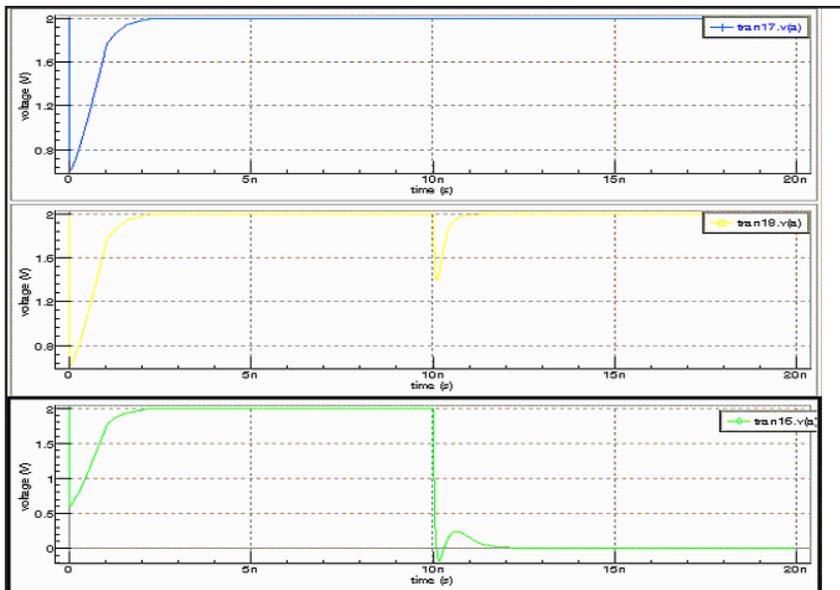


Figure 13. Latch circuit behavior affected by incoming single event upset particle.