

## CUSTOM IC CAD PRODUCT LINE



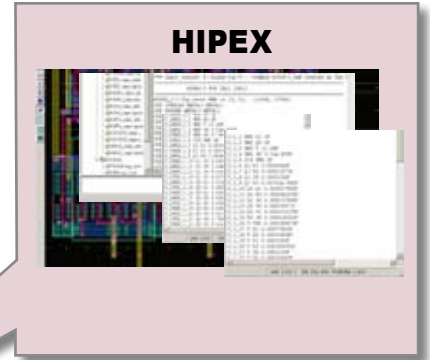
**IC layout, DRC/LVS verification, and RC parasitic extraction environment for analog, mixed-signal and RF design engineers**



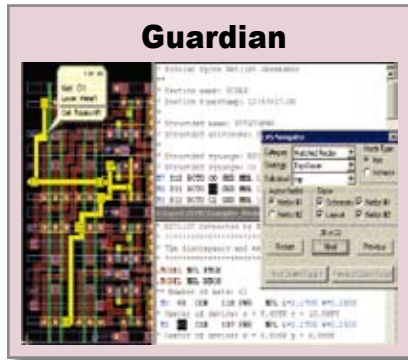
# CELEBRITY



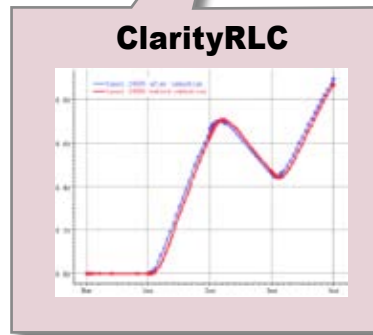
LAYOUT EDITOR



FULL-CHIP PARASITIC EXTRACTION



DRC/LVS/NET PHYSICAL VERIFICATION



RLC NETLIST REDUCTION

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