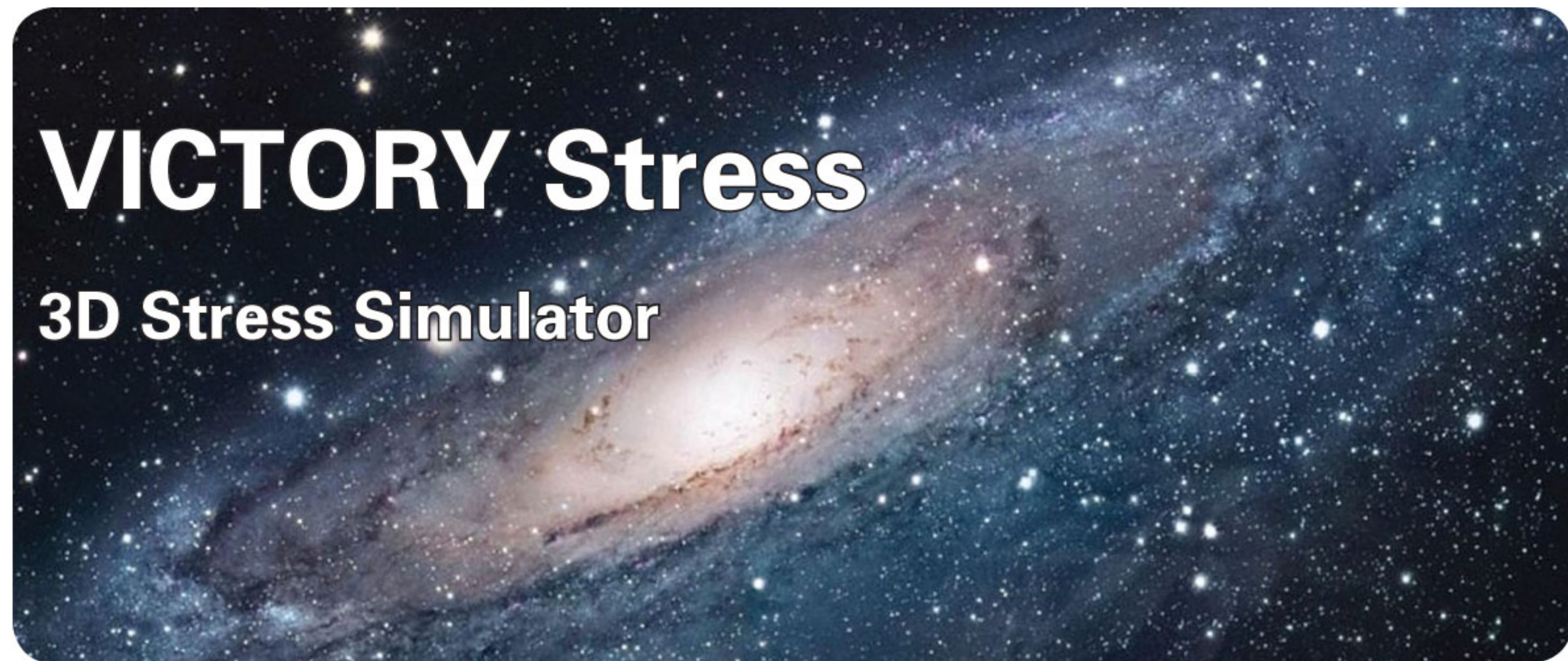
3D Stress Simulation Solutions



Stress Simulation for FinFET Devices

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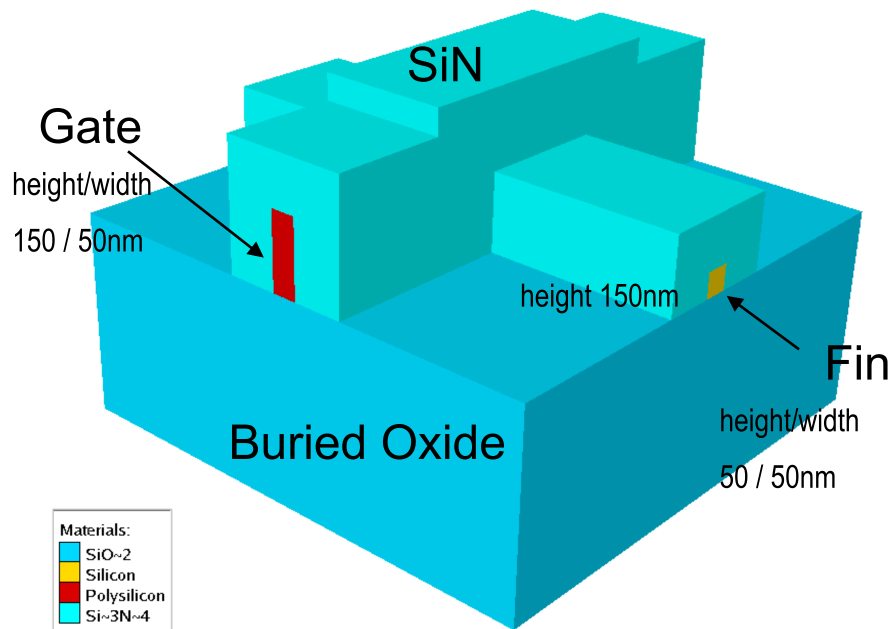
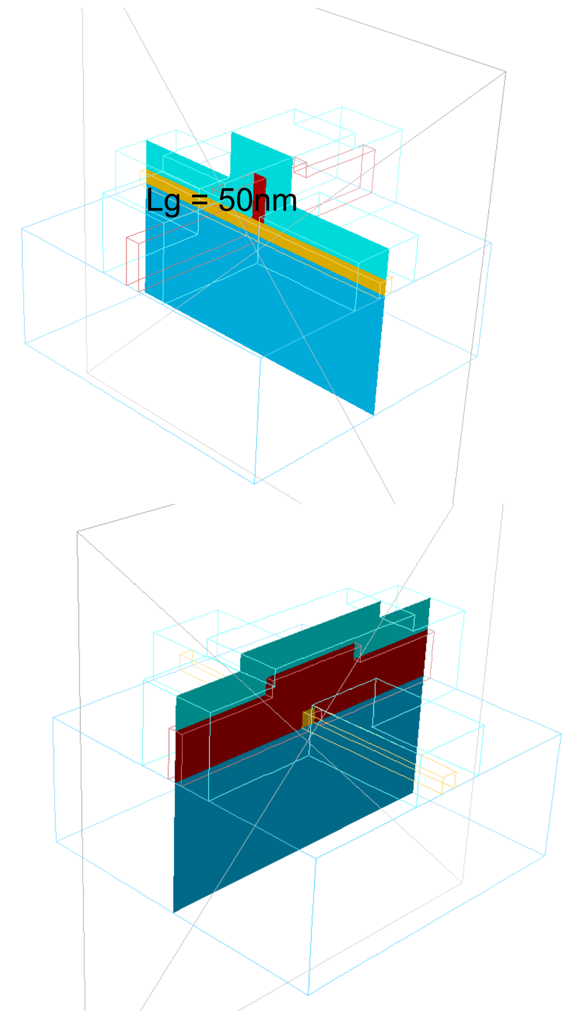
Introduction

- VICTORY Stress provides a complete solution for analysis of 3D anisotropic stress in crystalline silicon
- Stress simulation can be performed over the device structure in whole or in part
- It accounts for all isotropic and anisotropic properties of the materials, boundaries and initial conditions
- “Design of Experiments” with VWF can be used to analyze stress dependence on process parameters such as gate length or thickness variations

FinFET Nominal Device Structure





Nominal 50nm 3D FinFET structure. Buried Oxide thickness is fixed at 400nm. Fin width, height and gate length are varied according to Table I.

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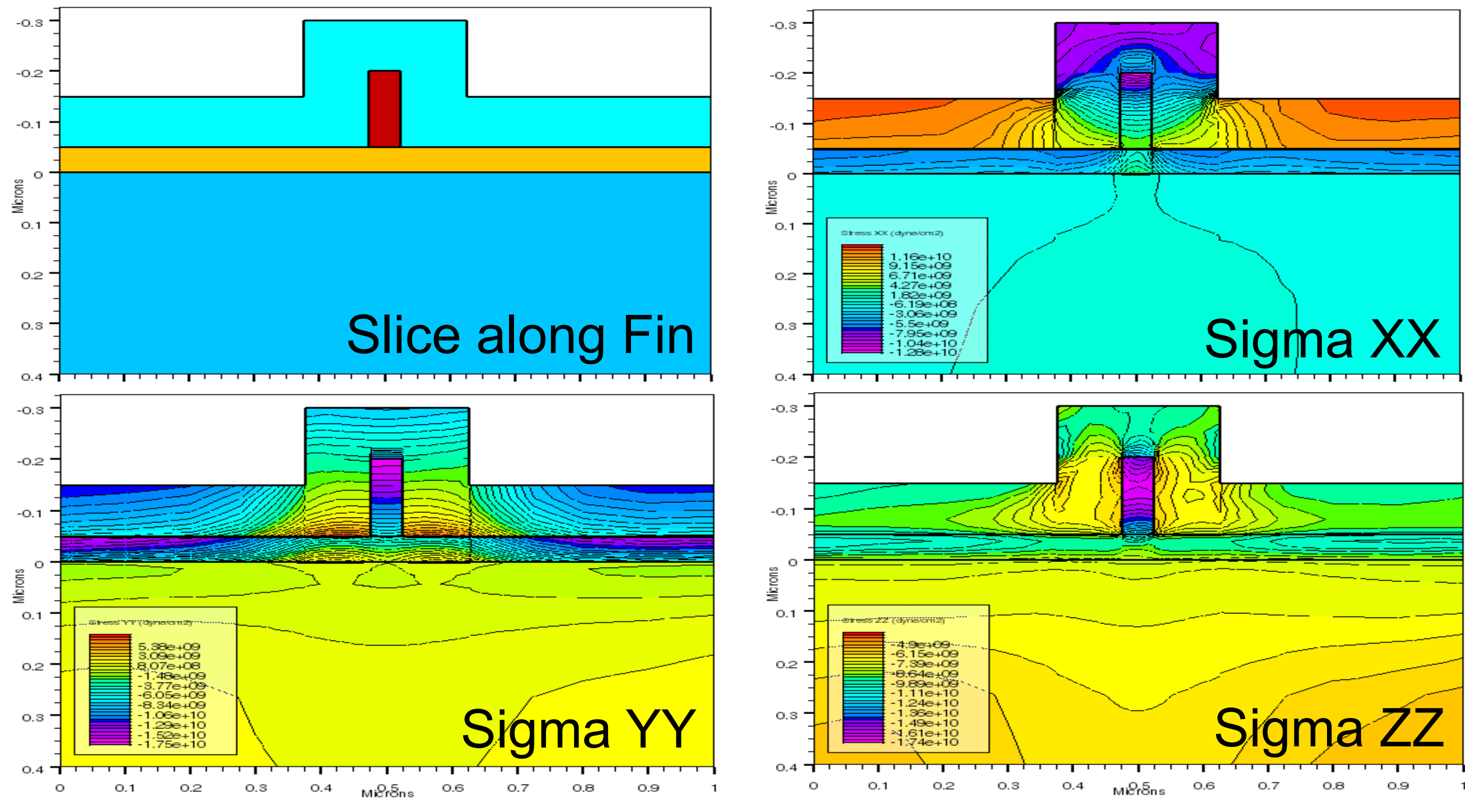
FinFET Stress Distribution



Stress distribution in FinFET channel under tensile stress from nitride capping layer.

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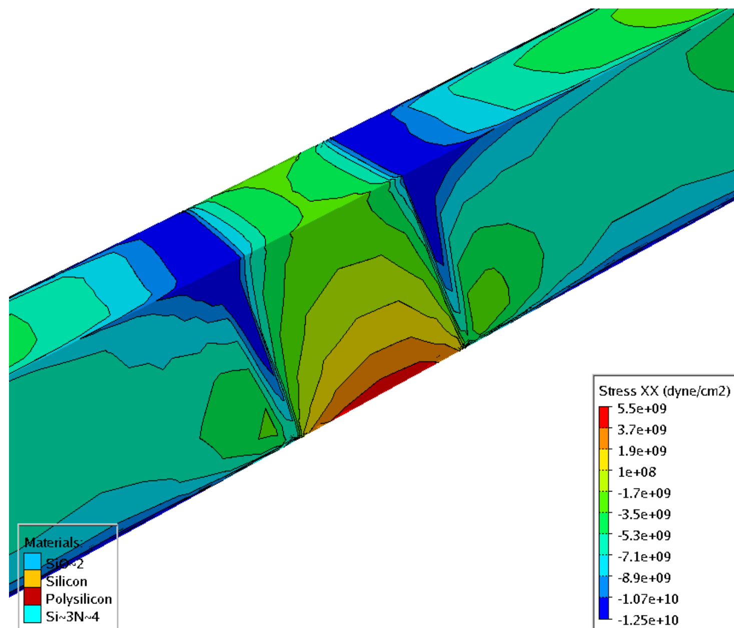
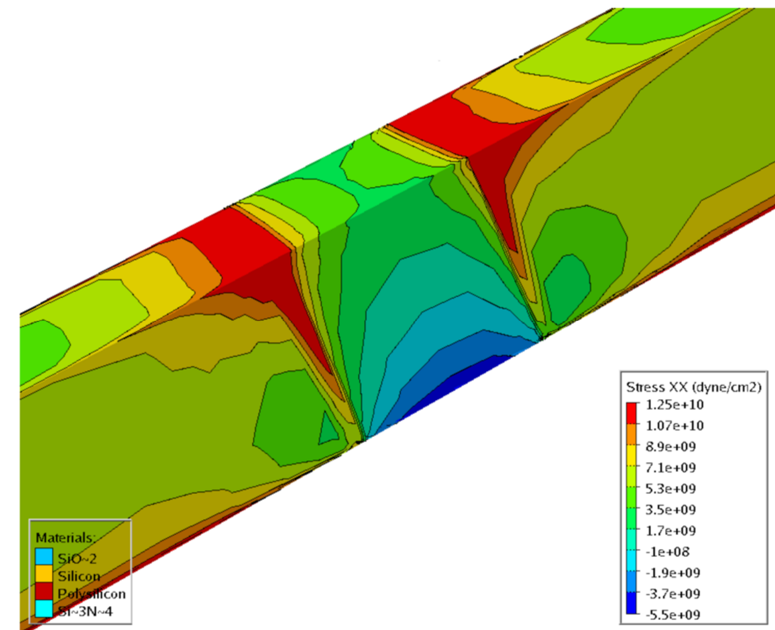
3D Stress Distribution in FinFET Channel

Channel under tensile stress



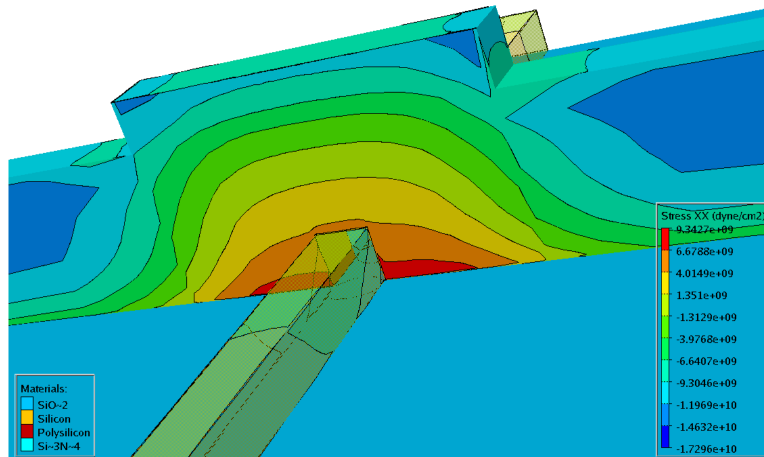
Channel under compressive stress



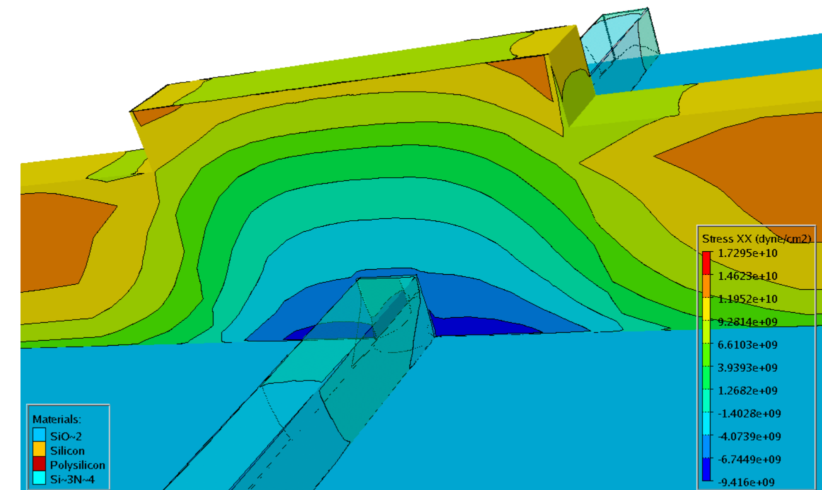
3D stress contour profiles along the channel in the <100> fin direction.

3D Stress Distribution in the FinFET

FinFET under tensile stress



FinFET under compressive stress



3D contour profiles showing stress distribution in the polysilicon gate.

Geometrical Parameter Variations Used in DOE

50nm 100nm 250nm 500nm

Gate length variation →

50nm 75nm 150nm 300nm

Gate height variation →

3D FinFET structures showing gate length and height variations.
Silicon nitride capping layer is not shown.

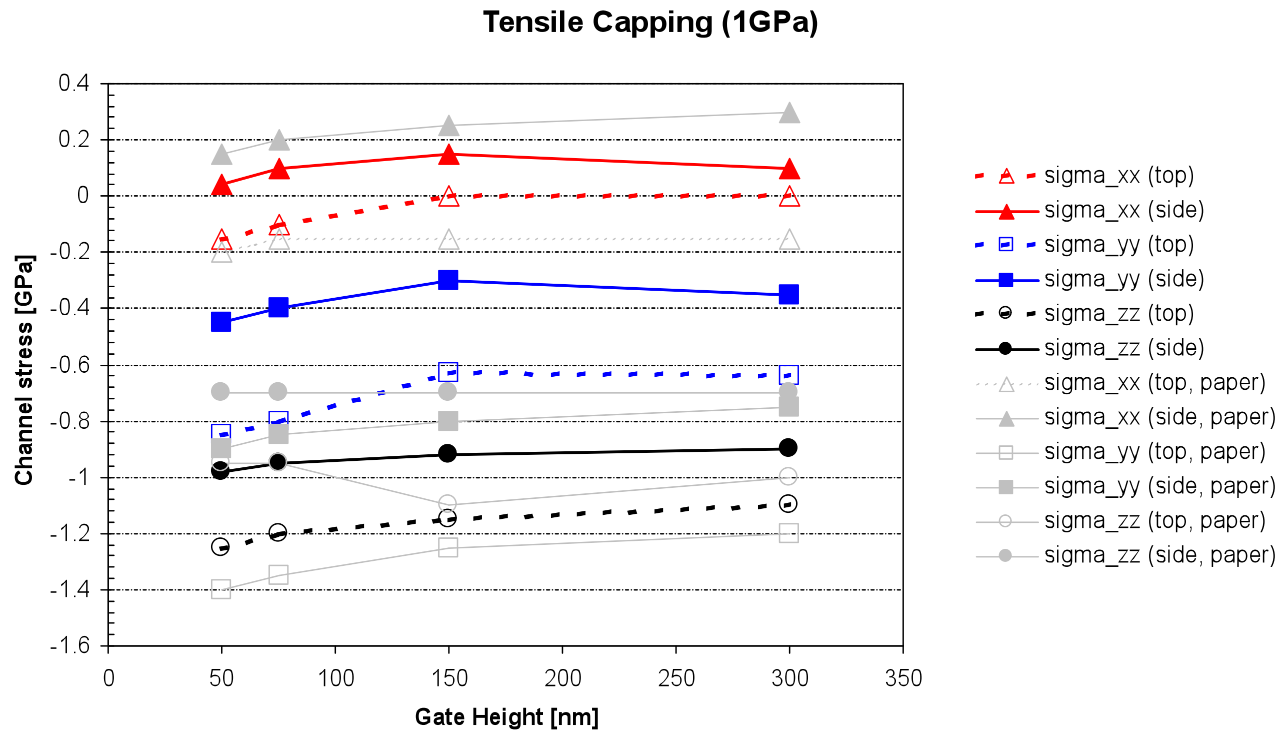
FinFET Geometrical Parameters

Table I. Geometrical parameter variations used in this case study

	$\langle 100 \rangle$ Nominal	$\langle 100 \rangle$ HAR	$\langle 110 \rangle$ Nominal	$\langle 110 \rangle$ HAR
T_{SiN} [nm]	100	100	100	100
W_{Fin} [nm]	50	25	50	25
T_{Fin} [nm]	50	100	50	100
L_g [nm]	50	50	50	50
T_{Gate} [nm]	150	150	150	150
T_{BOX} [nm]	400	400	400	400
Orientation	$\langle 100 \rangle$	$\langle 100 \rangle$	$\langle 110 \rangle$	$\langle 110 \rangle$

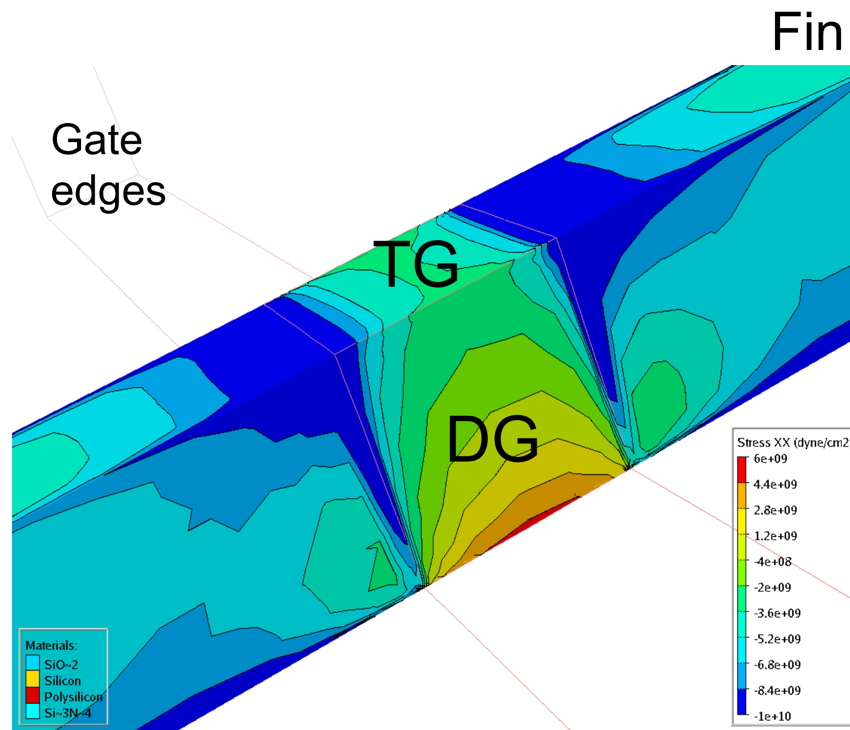
HAR – High Aspect Ratio (Gate Height to Length)

Impact of Gate Height Variation on Stress



Tensile capping layer (1GPa) is applied to varying gate heights on <100> structures. *Reference data from paper [1] are depicted in gray.*

Explanation of “TG” & “DG” Symbols



Sidewall-surface stress values are listed under “DG”; top-surface stress values are listed under “TG”. *“DG” stands for double-gate FinFET, and “TG” for tri-gate FinFET. When calculating mobility enhancement, double-gate are calculated from the “DG” stress values, while tri-gate are calculated from weighted 1/3”TG” and 2/3”DG” stress values*

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Mobility Enhancement Piezoresistivity Model

Piezoresistivity constants for different wafer orientation used for mobility enhancement evaluation, [2,3], in VICTORY Stress simulation

Material	n-type		p-type	
10^{-12} $cm^2/dyne$	<100>	<110>	<100>	<110>
π_{11}	-102.2	-31.1	6.6	71.8
π_{12}	53.4	-17.5	-1.1	-66.3
π_{13}	53.4	53.4	-1.1	-1.1

Mobility enhancement factors are calculated by use of average stress values and piezoresistivity factors.

$$\frac{\Delta\mu_{xx}^{DG}}{\mu} = (1+\pi_{11}\sigma_{xx})\times(1+\pi_{12}\sigma_{yy})\times(1+\pi_{13}\sigma_{zz})-1$$

$$\frac{\Delta\mu_{xx}^{TG}}{\mu} = \frac{2}{3}\frac{\Delta\mu_{xx}^{DG}}{\mu} + \frac{1}{3}\left[(1+\pi_{11}\sigma_{xx})\times(1+\pi_{12}\sigma_{yy})\times(1+\pi_{13}\sigma_{zz})-1\right]$$

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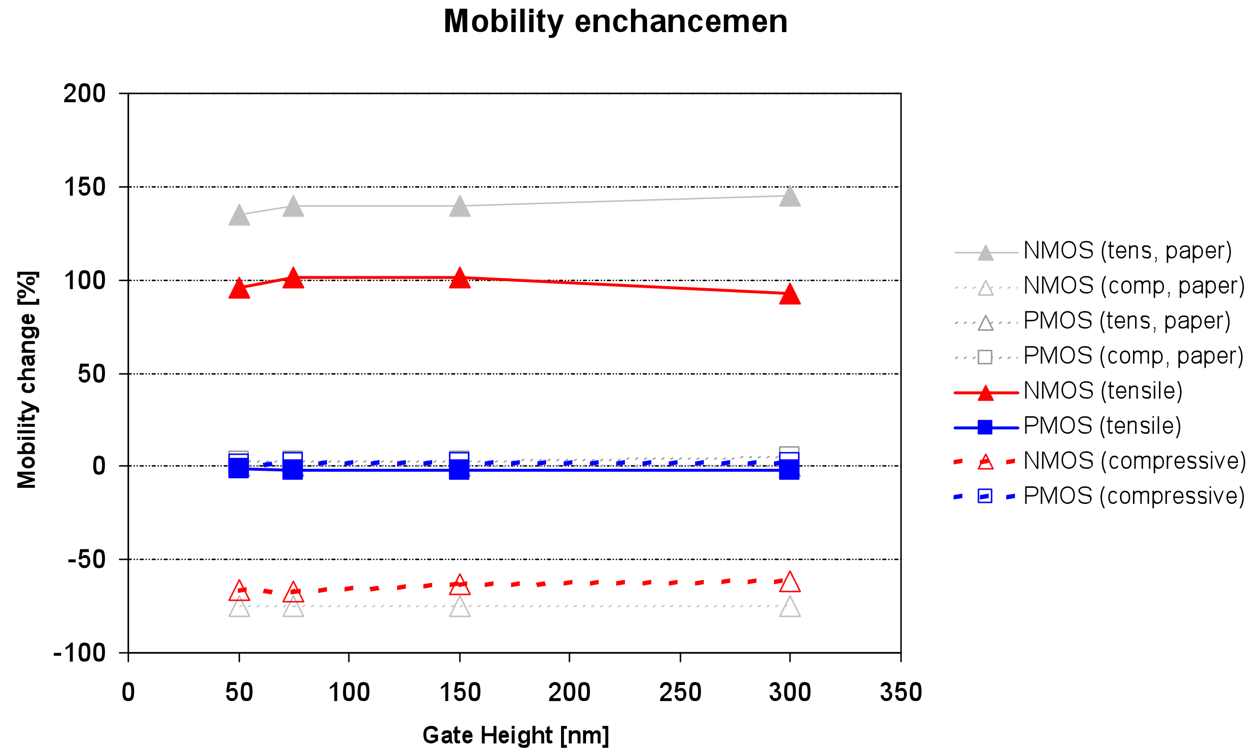
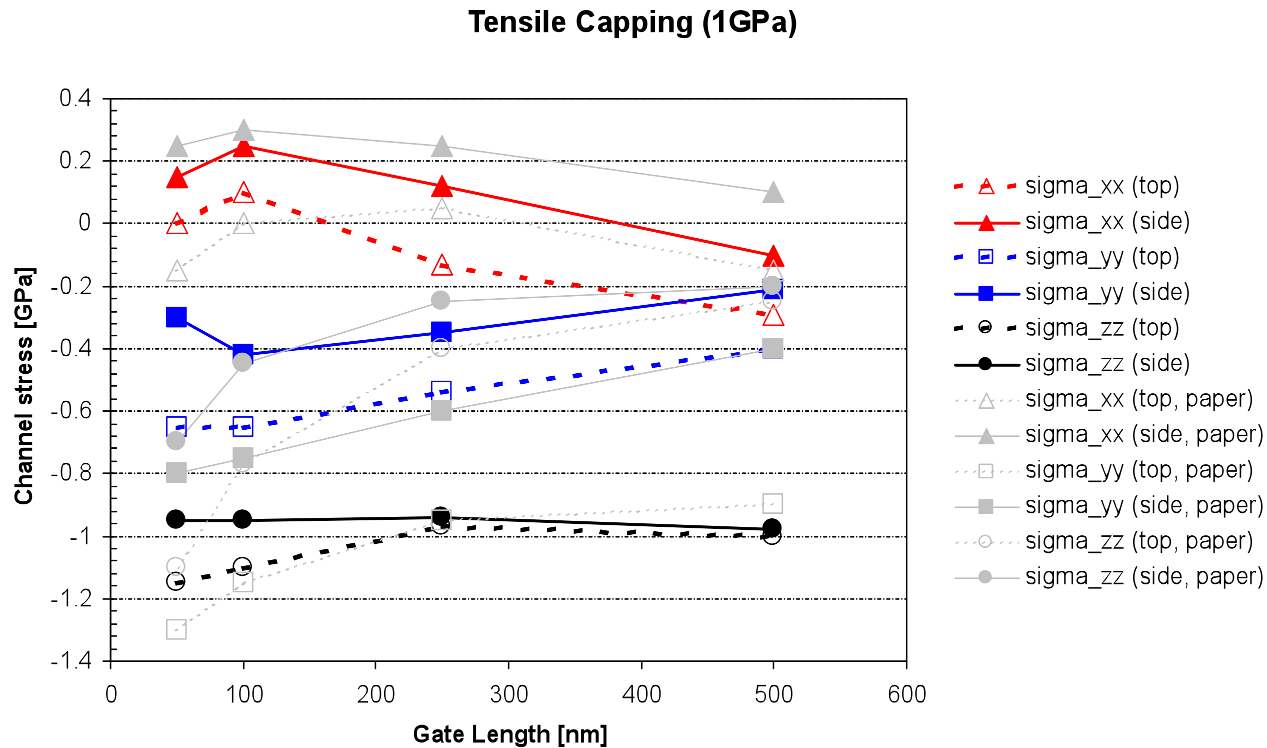
Impact of Gate Height Variation on Mobility



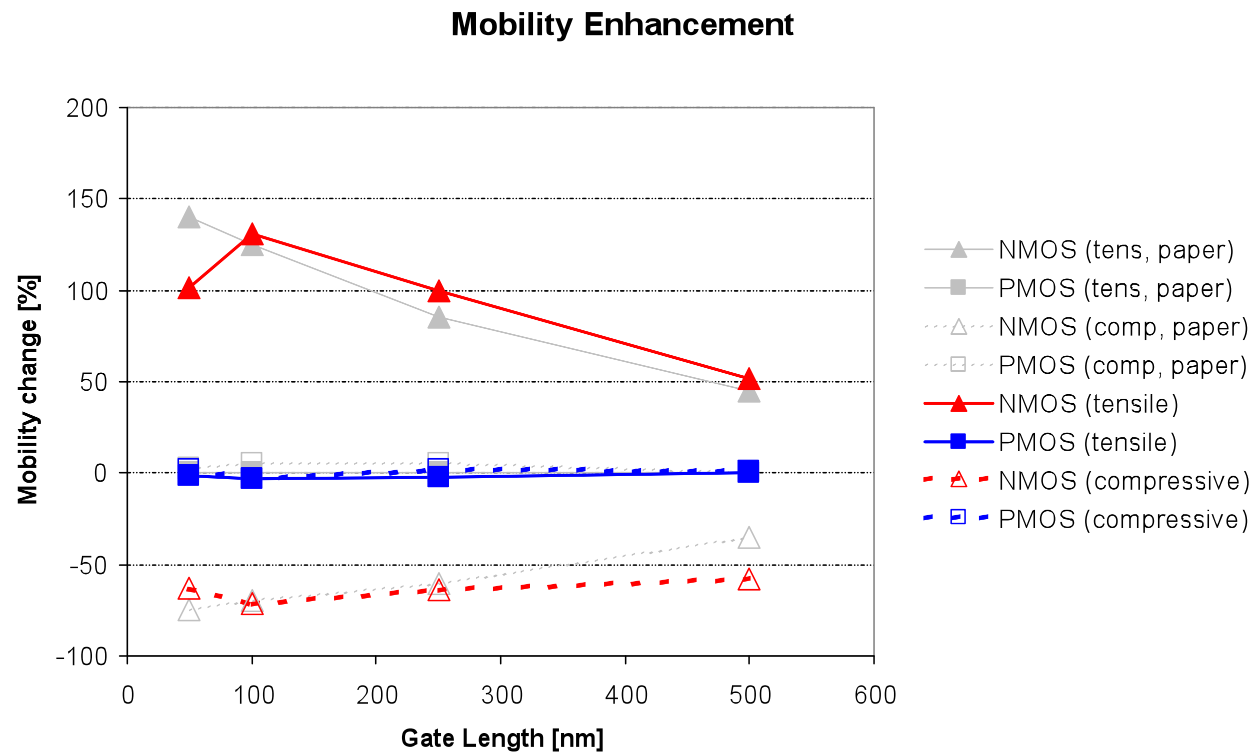
Gate height effect on DG mobility enhancement for <100> nominal structure with various gate thicknesses. *Reference data from paper [1] are depicted in gray.*

Impact of Gate Length Variation on Stress



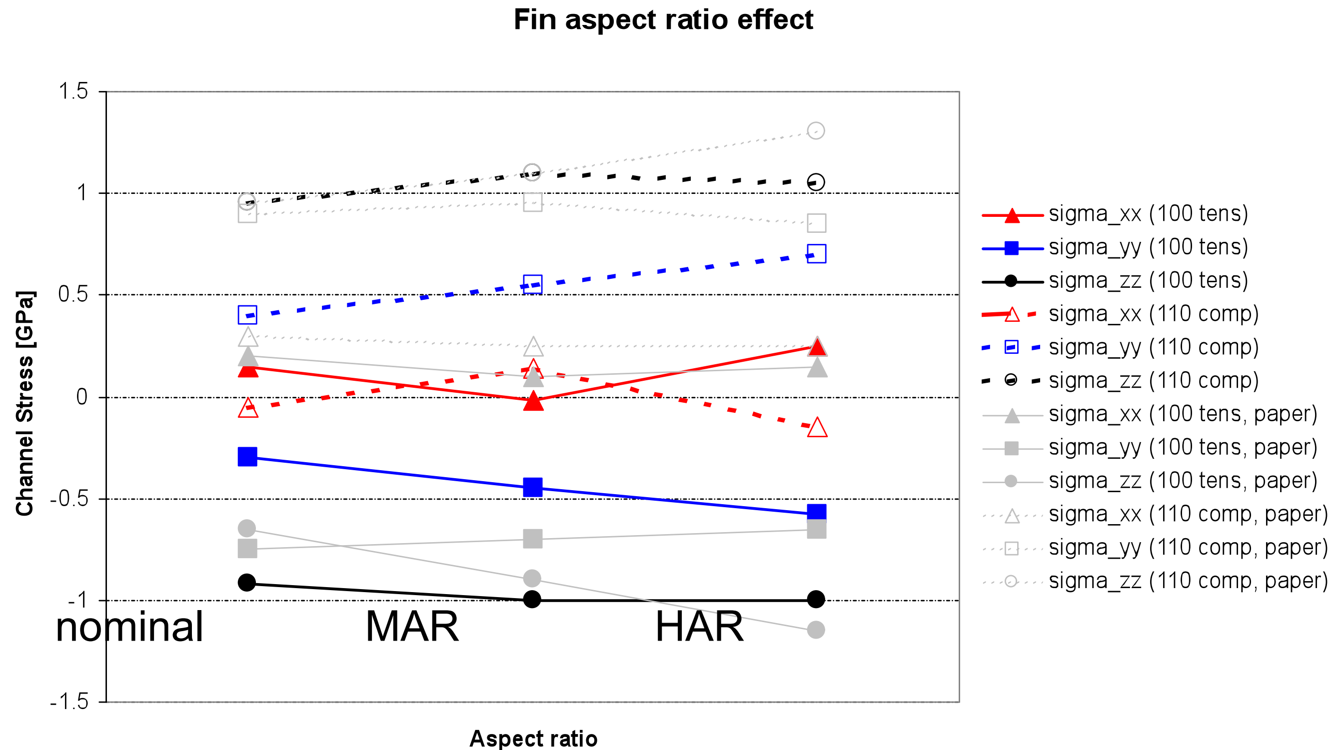
Tensile capping layer of 1GPa is applied for <100> nominal structure with various gate lengths. *Reference data from paper [1] are depicted in gray.*

Impact of Gate Length Variation on Mobility



Gate length effect on DG mobility enhancement for <100> nominal structure with various gate lengths. *Reference data from paper [1] are depicted in gray.*

Impact of Fin Aspect Ratio Variation on Stress

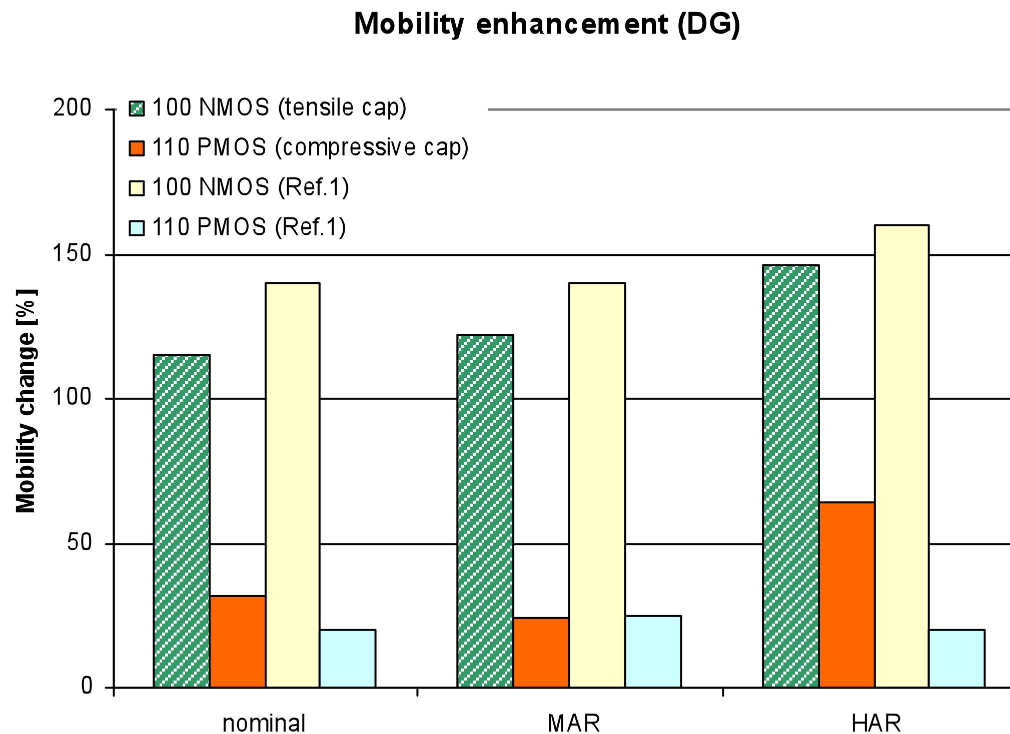


1GPa tensile capping layer is used for (100)-sidewall fins and –1GPa compressive capping layer is used for (110)-sidewall fins. Aspect ratios are given in Table I.

Reference data from paper [1] are depicted in gray.

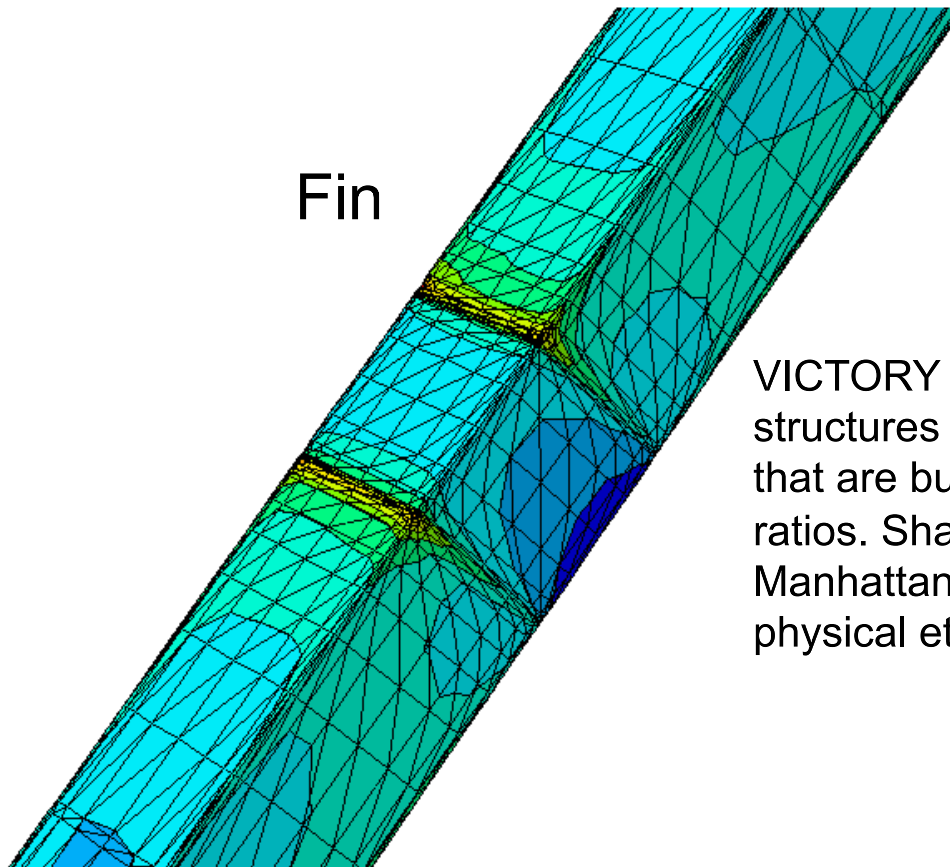
MAR – Medium Aspect Ratio (Gate Height to Length)

Impact of Fin Aspect Ratio Variation on Mobility



Fin aspect ratio effect on DG mobility enhancement for <100> NMOS with 1GPa tensile capping layer and <110> PMOS with –1GPa compressive capping layer.

Mesh in the Active Area



VICTORY Stress mesh is suitable for structures found in modern technologies that are built on small sizes and high aspect ratios. Shapes of Fin could be of a Manhattan type or rounded due to realistic physical etch and deposition.

References

1. Kyougsub Shin, Chi On Chui and Tsu-Jae King. Dual Stress Capping Layer Enhancement Study for Hybrid Orientation FinFET CMOS Technology. IEEE, 2005,
2. T. Manku and A. Nathan. Valence energy-band structure for strained group –IV semiconductors, JAP, 1993, 73(3), 1205.
3. Yozo Kanda. A Graphical Representation of the Piezoresistance Coefficients in Silicon. IEEE Trans. Electron Device, 1982, ED-29, 64